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Quantifying non-uniform InP-on-Si wafer expansion with a sub-50 nm precision using E-beam metrology

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Abstract Text: The non-uniform expansion of InP layers bonded directly and with the adhesive-BCB to 2" silicon substrates is quantified and compared on a 2" wafer-scale by using E-beam as metrology tool with a sub-50 nm precision.

Wafer-scale bonding for the integration of III-V semiconductor material layer on silicon substrate is an important technological aspect in realizing on-chip components for optical interconnects, such as light sources, modulators, detectors, etc. [1]. Despite this importance, there is little experimental verification available on how the bonded layer responds to the processing parameters, in particular temperature, especially on the wafer-scale. The predictable temperature expansion behaviour is critically important when fabricating devices requiring high-precision alignment between different layers [2]. In this work, we address the aforementioned issues by using E-beam as metrology tool to examine the expansion non-uniformities of InP layer bonded to 2" silicon substrate using two different methods: adhesive bonding and direct bonding with the intermediate Al_2O_3 layer [3].

Wafer expansion is determined by scanning an array of alignment marks across the wafer, which were first defined on a resist layer with the same E-beam lithography tool, followed by the transfer to the InP layer using dry or wet etching. Two different bonding approaches were utilized, which are transferrable to process flows used for fabricating semiconductor on-chip devices. In case of the adhesive BCB (Benzocyclobutene)-based bonding, the crosses were first transferred to the InP wafer, which was then bonded to Si/SiO₂ in a wafer bonder at 250 °C, and finally the crosses were opened from the other side by removing the InP substrate and the etch-stop layer (the equivalent of the double-sided processing). The metrological measurements show significant non-uniform distortion in the bonded InP layer observed as changes in the positions of crosses (Fig. 1, *left*). In case of the direct bonding approach, a thin ALD Al_2O_3 layer was deposited on both the InP and Si/SiO₂ wafers before placing them on top of each other for pre-bonding. The wafers were then thermally annealed in the wafer bonder at 300°C, and after the removal of the InP substrate and the etch-stop layer the transfer of crosses was performed on already bonded sample (the equivalent of the single-sided processing). Much less of non-uniform distortion is observed across the bonded InP layer (Fig. 1, *right*). No further considerable non-uniform expansion is observed for the BCB bonded sample after rapid thermal annealing performed at 420°C for a few seconds, meanwhile the directly bonded sample shows no further expansion even after annealing at 650°C for 15 min in the phosphine atmosphere. This result verifies that InP regrowth can be performed on the directly bonded sample.

The expansion observed in the bonded InP layers explains the misalignment that appears between the buried heterostructure and the photonic crystal cavities in our fabricated laser devices (Fig. 2). The results bear an important significance in effort to increase the alignment accuracy necessary for the optimal laser performance.

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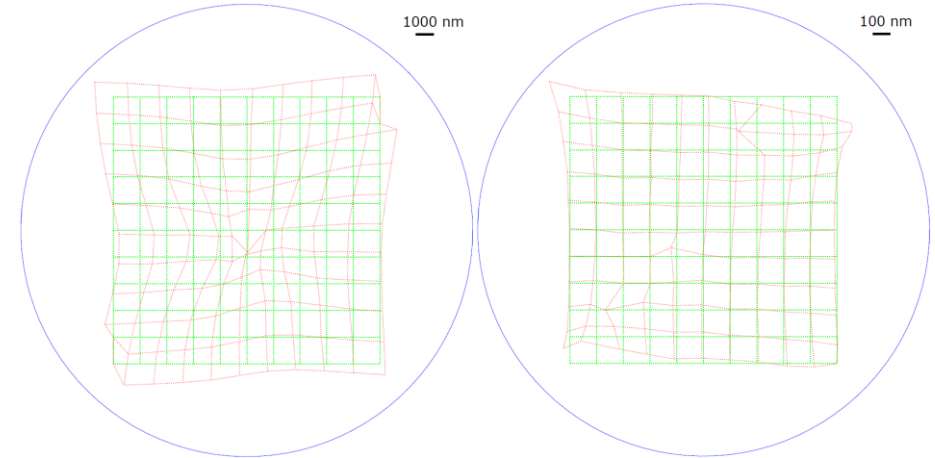


Figure 1. Distortion maps representing non-uniform InP-on-Si wafer expansion as measured by E-beam used as metrological SEM. *Left*: double-sided processing approach with BCB bonding. *Right*: single-sided processing approach with direct wafer bonding. Blue circles indicate the outline of a 2" wafer; green grid represents initially exposed pattern of alignment marks; red grid represents measured positions of alignment marks after fabrication. The scale bar is for the differences between these two grids. A uniform linear expansion has been subtracted from both maps to minimize distortion.

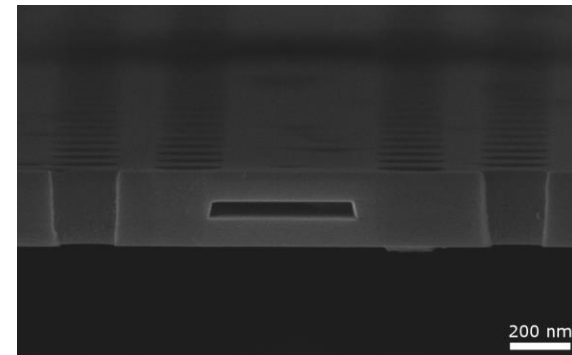


Figure 2. Cross-sectional SEM image of the selectively wet-etched buried gain material inside the InP photonic crystal membrane directly bonded to silicon substrate.